MODEL BASED DESIGN OF AN AVIONICS POWER LINE COMMUNICATIONS PHYSICAL LAYER

Juergen Wassner, Stephen Dominiak, Javier Moya
Lucerne University of Applied Sciences & Arts, Lucerne, Switzerland

Abstract

Transmitting data over the aircraft power distribution network using Power Line Communications (PLC) technology provides an interesting solution for providing significant aircraft wiring weight, volume and complexity savings. A PLC protocol dedicated for real-time, safety-critical applications has been developed. The physical layer of the protocol is based on the international IEEE 1901 standard. An overview of the advanced digital signal processing techniques required to provide robust communications over the harsh power line communications channel is provided. In order to cope with the complexity in the realization of the physical layer, a process using model based design based on concepts from DO-254 and DO-331 is proposed. This process is used for the hardware-based design and verification of the PLC protocol.

Introduction

The More Electric Aircraft (MEA) trend has led to hydraulic and pneumatic systems being replaced with electric systems. Control of these electrical systems requires additional data networks within the aircraft which leads to increased complexity, weight and volume in aircraft wiring. In fact some reports show as much as 40% of the electrical wiring in the aircraft can be attributed to data network wiring [1].

One potential solution for reducing the amount of aircraft wiring is the use of Power Line Communications (PLC) in which data is transmitted over the aircraft power network. This allows the data network to be eliminated which can provide significant wiring complexity, weight and volume savings and will also reduce the necessary installation and maintenance effort. The potential application of PLC for avionics is not new and previous work within the EC FP7 TAUPE project has validated the technology up to a Technology Readiness Level (TRL) of 4 [2]. Nevertheless the previous investigation was based on the use of commercial PLC technology and certain deficiencies with that technology had been identified [2]. Furthermore the relatively small market segment provided by aeronautics (compared to the consumer market) results in a general lack of support for any necessary adaptations to the commercial technology by the technology suppliers. Based on the need for a PLC technology to support the requirements of safety-critical, real-time applications not only in avionics, but also in other niche market areas, the development of a dedicated PLC solution was started at Lucerne University of Applied Sciences and Arts (HSLU) in 2012. The main design goals for the PLC protocol are to maximize reliability, reduce latency and to provide deterministic behavior. These goals are different from commercial technology which includes much dynamic behavior in order to support plug-and-play and high bandwidth applications. The HSLU PLC solution not only targets a communications protocol which meets the necessary functional and performance requirements, but also provides design assurance as is required for safety-critical applications.

As will be described within this paper providing reliable communications over the harsh power line communications channel requires the use of advanced Digital Signal Processing (DSP) algorithms at the physical layer (PHY) of the PLC protocol. In order to cope with the inherent complexity as well as time and cost in the design and development of these algorithms, the concept of Model Based Design (MBD) is used. The focus of this paper is to present certain aspects of the PLC PHY as well as the MBD process used in the design and Verification and Validation (V&V) processes.

PLC Transmission Channel

Transmitting data over the aircraft Power Distribution Network (PDN) does not come without its challenges. The PDN has been optimized for the

distribution of a very low-frequency power signal and is rather unsuitable for high-speed data communications. The following main factors differentiate the wiring of the PDN from the wiring typically found in data networks.

- PDN wiring is unshielded.
- PDN wiring will not consist of a twisted-pair but will usually either consist of a single-wire with return over the aircraft chassis or several wires routed in parallel for 3-phase systems. This often leads to a highly asymmetric transmission medium.
- The PDN topology is often tree-like and contains a number of branches or other points at which impedance discontinuities will occur with impedances varying between a few ohms to a few kiloohms [3].
- The impedance of loads attached to the PDN is optimized for the maximum power transfer of the power signal and is rather arbitrary for higher frequencies.
- Power conversion and other active power elements within loads will generate static and transient noise which will be conducted or even coupled from external sources onto the PDN.

These characteristics lead to a less than ideal communications channel. Impedance mismatches will exist at the loads, branching points and other connection points throughout the PDN. Each impedance discontinuity will lead to a partial transmission and partial reflection of the PLC signal. At branches the signal power will be split with partial transmission of signal "echoes" down each of the branches. At the receiver these different echoes and reflections will combine leading to highly frequency selective attenuation. Several "notches" or narrow bands which suffer from higher attenuation than adjacent bands will be present. This effect is commonly referred to as multipath. As the paths and load impedances between any two transmitters and receivers will vary, so too will the transmission channels vary. This means that the communications channel has a strong dependence upon the location of the transmitter and receiver. Figure 1 shows two typical PLC communications channels which have been measured at different locations on a test bench of the Airbus A380 Cabin Lighting System within the EC FP7 TAUPE project. As can be seen a few deep notches are present along with several more moderate notches. It is also apparent that the mean attenuation increases versus frequency which is mainly due to the skin effect and dielectric losses from the insulating material [4].

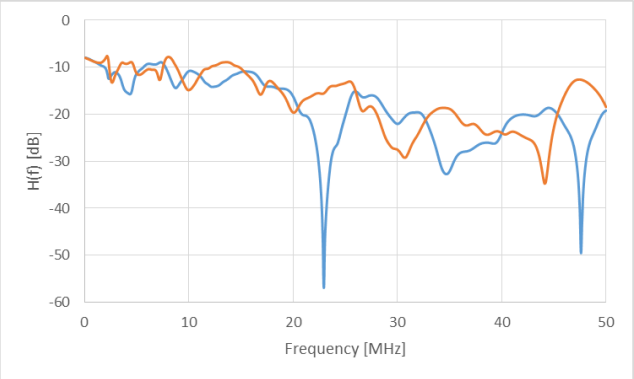

Figure 1: Example PLC channel transfer function

It is a well-accepted fact that the noise on a power line does not have properties of a "white" Gaussian noise. Typically three general classes of noise can be expected:

- Colored background noise with a higher Power Spectral Density (PSD) at lower frequencies.
- Narrowband background noises which may result from external sources (e.g. broadcast radio) or system internal sources (e.g. application device clock signal)
- Impulsive noise which may be generated from multiple sources at the loads including on/off switching behavior, switched power supplies, etc.

Furthermore the lack of a shield or twisting of the power cables means that the isolation from external effects which may be electro-magnetically coupled onto the power line is reduced. External sources of noise can be other aircraft systems operating within the same (or a nearby) wiring harness, High Intensity Radiated Fields (HIRF) from broadcast radio, low-frequency voltage spikes, lightning, etc.

The main factor influencing the performance of any communication system is the Signal-to-Noise-

Ratio (SNR) present at the receiver. Therefore even in environments with high channel attenuation or high noise, an increase in the transmission signal power could still provide a sufficient SNR. However, within the aircraft environment the emissions of all devices within the PLC signal frequency range (2-50MHz) is strictly regulated through limits imposed by RTCA DO-160. Even though PLC provides intentional emissions within this band, from the EMC point-of-view it must be categorized as unintentional emissions or noise. These limits mean that the transmission PSD of the PLC signal must be limited in order to be in compliance with the limit for the relevant environmental category.

The fact that the PLC signal propagates over a fixed wiring network means that the channel will exhibit a certain amount of determinism [5]. This is especially true within the aircraft in which the PDN specification is well documented. In fact time-varying behavior in an installed avionics PLC system would only result from the time-varying impedances of loads or switching within the network. Proper filter and coupler design can provide a solution which reduces the influence of application device impedance changes on the PLC channel, thereby providing less time-varying behavior. This sets PLC apart from wireless, which sometimes is being considered alongside PLC as a communications technology. However, the dynamic propagation environment of a wireless signal poses a significant challenge for the use of the technology in safety-critical applications due to the highly random and time-varying nature of the wireless channel. The determinism provided by PLC is considered to be one of the main advantages for the use of PLC over wireless technology.

PLC Physical Layer

Overview

According to the OSI reference model the physical layer (PHY) is responsible for the transparent transmission of bit streams across physical connections [6]. It is actually through advanced DSP techniques within the PHY that the majority of the challenges presented in the previous section related to the transmission channel will be mitigated. None of the characteristics for PLC previously mentioned are unique to the avionics environment and they generally exist in all environments in which PLC is used. The PLC technology has been developed and optimized for similar environmental conditions for over 15 years now. For the majority of that time PLC suffered from the lack of international standards and many industry or proprietary solutions were available. In 2010 that has changed with the approval of two international standards: IEEE 1901 and ITU G.hn (G.9960/G.9961). The use of a standardized solution has a benefit in terms of the experience gained through other market areas as well as the economic benefits from the potential for multiple technology suppliers. After a detailed analysis, the IEEE 1901 standard was selected as the basis for the HSLU PLC solution. An overview of the architecture of the PLC transceiver which includes the PHY transmitter and PHY receiver is shown in Figure 2. The PHY transmitter is responsible for converting the PLC MAC frame provided by the Data Link Layer (DLL) into a PLC signal waveform suitable for transmission on the power line medium. The PHY receiver on the other hand decodes the PLC signal waveform into a MAC frame which is passed to the DLL. The Analog Front End (AFE) provides Digital-to-Analog, Analog-to-Digital and amplification functionality for the analog signal. The coupler is responsible superimposing the high-power, low-frequency power signal with the low-power, high-frequency PLC signal on the power line. The main components of the PLC PHY will now be described within this section.

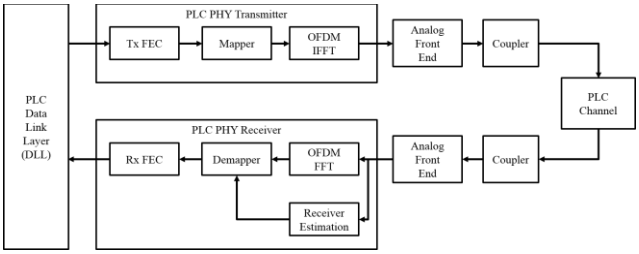

Figure 2: PLC Transceiver Architecture

Orthogonal Frequency Division Multiplexing

The core modulation technique around which the PLC PHY is designed is known as Orthogonal Frequency Division Multiplexing (OFDM). With OFDM the overall signal spectrum is divided into a number of closely spaced, orthogonal channels and data is modulated onto those different channels and

transmitted in parallel. In other words the input serial bit stream will be translated to a number of parallel frequency sub-carriers at the transmitter. The fact that the adjacent sub-channels are orthogonal means that a very close spacing can be achieved which leads to a high spectral efficiency. At the receiver the parallel sub-carriers will again be translated into a serial bit stream. The OFDM functionality is realized with the Inverse Fast Fourier Transformer (IFFT) algorithm at the transmitter and the FFT algorithm at the receiver. With OFDM the highly frequency selective PLC broadband channel is transformed into a number of "flat" narrowband channels. This greatly reduces the complexity of channel equalization. The overall OFDM symbol is then sent at a lower sample rate compared to what would be required for single-carrier systems with the same bandwidth. The previously mentioned multipath channel could potentially lead to Inter-Symbol-Interference (ISI) as different echoes arrive at different times, which depredates the performance. In order to mitigate this, a Guard Interval (GI) is inserted at the beginning of the OFDM symbol. As long as the GI is selected to be longer than the signal delay spread, no ISI will occur.

According to IEEE 1901 the PLC signal is a baseband OFDM signal consisting of up to 2048 sub-carriers between 0-50 MHz. With the recommended PHY sample rate of 100 MHz this leads to a sub-carrier spacing of approx. 24.414 kHz. Investigations have shown that the coherence bandwidth of the aircraft PLC channel is more than sufficient for the sub-carrier channel to be considered as flat [7]. As the overall noise on the power line and also the number of potential HIRF sources is higher for frequencies below 2 MHz, those sub-carriers will be disabled. This also leaves a sufficient margin for filtering any effects from voltage spikes or other low-frequency interferers (e.g. audio).

Mapper/Demapper

A further advantage of OFDM is that each sub-carrier may be individually modulated through a mapping function in the transmitter and then de-modulated through a corresponding demapping function at the receiver. Each sub-carrier can be configured individually according to the following parameters:

- Active/Inactive: Sub-carriers may be activated or deactivated. No data will be mapped to inactive sub-carriers and no output power will be transmitted on those sub-carriers.
- IQ Modulation: Different Phase Shift Keying (PSK) or Quadrature Amplitude Modulation (QAM) constellation size may be selected which define the number of bits that can be mapped to each symbol. The IEEE 1901 standard defines constellations for up to 12 bits per symbol. However for robust communications only 1, 2, 3 or 4 bits per symbol (BPSK, QPSK, 8-QAM or 16-QAM) have been found to be suitable.
- Output power amplitude: A digital attenuation that may be applied to sub-carriers in order to reduce the PSD transmitted on that sub-carrier.

These features allow the overall output PSD of the PLC signal to be tuned according to the relevant EMC guidelines or system requirements as well as adapting the modulation used on each sub-carrier for individual communications channels. The latter, commonly known as adaptive bit-loading, can be used to optimize the achievable data rate for the given channel capacity of a frequency selective channel. However, it requires measurements of the channel to be performed and then both a feedback and control channel such that measurements may be propagated from the receiver to the transmitter and a common modulation between transmitter and receiver may be agreed upon. A typical algorithm for modulation selection is the water pouring method [8].

Performing bit-loading does suffers from a number of disadvantages including added protocol complexity, increased connection setup times and abrupt changes in the channel (e.g. due to load switching) lead to degraded performance until the bit-loading process converges again. Furthermore, it is not appropriate for one-to-many or broadcast communications. Bit-loading solutions lead to an optimum in terms of average capacity and error rate, however suffer from very poor worst case performance when transients exist in the network. The solution described in this paper targets an alternative approach in which the available potential

channel capacity is rather used to increase the system reliability. A common modulation is selected such that no feedback or control channels are required between the transmitter and receiver. This leads to a solution which provides predictable performance for both average as well as worst-case channel conditions.

Forward Error Correction

Forward Error Correction (FEC) is a common technique of adding redundant coding information at the transmitter which is then used at the receiver to correct bit errors due to channel deficiencies. As such it is a means to mitigate the negative effects of impulsive noise. FEC coding schemes must also be combined with interleaving in order to reduce the influence of burst errors by achieving a time and frequency distribution of the errors which can be better handled by the coding scheme. By using standard uncoded OFDM on a frequency selective PLC channel with impulsive noise, the overall error rate performance will be dominated by the sub-carriers containing the worst SNR. The use of interleaving and coding helps to ensure that the error rate is instead determined by the average SNR of all the sub-carriers [3]. It therefore plays a key role in the presented solution allowing sub-carriers containing a more favorable SNR to compensate for the negative effects of sub-carriers with a very low SNR, without having to dynamically adapt the used modulation and coding.

The FEC scheme is based on a Convolutional Turbo Code (CTC). Since their discovery turbo codes have seen widespread use in many communications standards as they provide performance near to the Shannon capacity [9]. As shown in Figure 3 FEC with CTC consists of three different operations at the transmitter. Scrambling helps to give the data a random distribution. Turbo Convolutional Encoding provides duo-binary encoding and supports code rates of either 1/2, 16/21 or 16/18 with block sizes of either 16, 136 or 520 bytes. After encoding the channel interleaving process provides bit-by-bit interleaving to ensure a suitable distribution of coding and information bits across the sub-carriers in the frequency domain. At the receiver descrambling and de-interleaving are simply reverse processes to those at the transmitter. Turbo Convolutional Decoding is an iterative process that uses soft-decisions obtained from demapping to derive binary values for each information bit. The process is based on a Maximum A-Posteriori (MAP) algorithm which is often estimated with the Max-Log-MAP algorithm, which has lower computational complexity. The number of decoder iterations becomes an important parameter with a trade-off between error-correcting performance and latency. However, multiple decoders may be implemented in parallel in order to reduce latency at the cost of more hardware resources. Another parameter to control the performance/resource tradeoff is the number of bits used to represent soft-decision inputs as well as branch and state metrics of the decoding trellis. A detailed analysis and performance evaluation has been performed to find reasonable values for all of these parameters.

One disadvantage of CTC compared to other coding schemes such as Reed-Solomon is that errors may only be corrected, but not directly detected. However, the presented PLC solution provides strong error detection through the use of an additional multi-layer Cyclic Redundancy Check (CRC). The detailed description of the CRC which is part of the DLL is outside the scope of this paper.

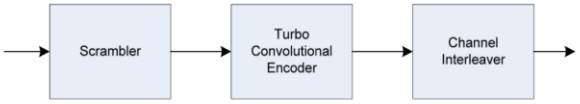

Figure 3: FEC Block Diagram

Receive Estimation and Equalization

The final major block of the PLC PHY transceiver is only present within the receiver. Two inherent issues necessary for the robust demodulation of data which must be solved at the receiver are channel estimation with equalization and frame synchronization. Channel Estimation (CE) and equalization is necessary in order to compensate for both the frequency-dependent attenuation as well as time-delay in the PLC channel. If a suitable estimate of both of these factors can be made, then through relatively simple equalization operations the frequency selective channel can be transformed into a series of flat sub-channels which can be reliably decoded through the OFDM FFT and demapper operations. Frame Synchronization (FS) is required in

order to synchronize the receiver processing onto the incoming sample stream. Both CE and FS are performed based on a known preamble which is sent at the beginning of each OFDM frame. The preamble consists of a series of repeating mini-symbols including a sign change in terms of the signal phase. Through a correlation and proper detection of the sign change, the end of the preamble can be very accurately detected. A comparison of the expected signal for the preamble mini-symbols against the received signal allows an accurate CE to be performed.

Furthermore, OFDM systems are rather sensitive to frequency offsets between the transmitter and receiver clock as it can lead to Inter-Carrier Interference (ICI) and a substantial performance degradation. Therefore an additional method is required at the receiver to compensate for such frequency offset such that drift effects and the amount of ICI may be minimized. In a standardized IEEE 1901 solution each node will synchronize its clock based on a beacon message sent by a master node in the network. However, the proposed solution provides a peer-to-peer architecture in which no master is present in order to avoid a potential single point-of-failure in the system. Therefore, an alternative frequency offset compensation concept is provided which is not dependent upon a single global clock. Frequency offset compensation is performed on a frame-by-frame basis.

Model Based Design

The design and development of the DSP algorithms as part of the PLC PHY presents a significant challenge. Although the PHY is based on the IEEE 1901 standard, unlike specifications for avionics data buses, many of the aspects of the implementation of IEEE 1901 are left open for proprietary design in order to allow for differentiating competition among technology suppliers. Furthermore many tradeoffs will exist in terms of hardware complexity, latency and performance. This means that a significant amount of design work still had to be performed. This challenge is compounded by the necessity for meeting the relevant Design Assurance Guidelines (DAG) if PLC is to be used for avionics systems. Due to the relatively high PLC signal bandwidth, which implies sampling frequencies of at least 100 MHz, and the advanced DSP requirements of IEEE 1901, the realization of the PHY has been targeted for hardware. Therefore, the relevant DAG is DO-254/ED-80. The most current version of the relevant software DAG, DO-178C, contains a supplement document specifically addressing Model-Based Development and Verification (DO-331) [10]. However, except for a few select references from the industry [11], to the best of the authors' knowledge no official guidance exists for applying MBD to DO-254. In addition to the design and verification processes, DO-254 also requires other processes such as planning, validation, configuration management. The focus of this paper is however on the design and verification and validation processes.

According to [10] a model can be considered as *an abstract representation of system used to support the development and verification process*. The following use-cases for MBD are also defined:

A. Provide unambiguous expression of requirements and architecture
B. Support the use of automated code generation
C. Support the use of automated test generation
D. Support the use of analysis tools for verification of requirements and architecture
E. Supporting the use of simulation for partial verification of requirements, architecture, and/or Executable Object Code

With two minor exceptions all of these use-cases for MBD of software can also be applied to the hardware process: A) DO-254 requires hardware design artifacts which are per definition not requirements and E) Executable Object Code may be substituted for the resulting hardware description code (VHDL).

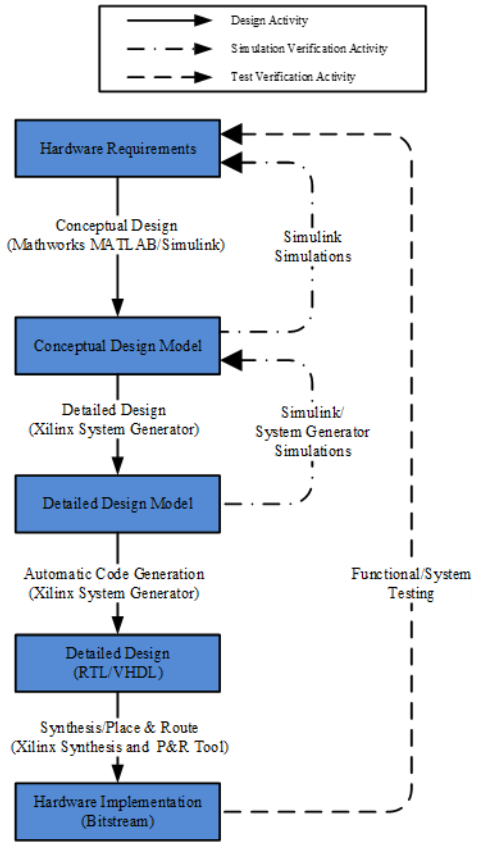

Figure 4: PLC PHY Design and V&V Process Overview

A design and V&V process for the PLC PHY has been defined based on concepts from DO-254 and DO-331 and is shown in Figure 4. The capture of textual hardware requirements serve as the beginning to the design process just as with a standard design (not based on MBD). However, the hardware design process is based around two different levels of models, a conceptual design model and a detailed design model. Both the conceptual design model and detailed design model are executable, meaning that simulations may be used in order to provide an initial two-step verification[1] of the design against the textual requirements before functional testing of the implementation on the hardware platform. Table 1 provides an overview of the different use-cases described earlier in this section which are used for the different levels of MBD. The conceptual and detailed design models will be described in more detail in the following sections.

Table 1: MBD Use-Cases for the Different Design Models of the PLC PHY

Model Type	MBD Use-Cases
Conceptual Design	A, E
Detailed Design	A, B, D, E

Conceptual Design Models

The conceptual design model provides a high-level abstraction of each of the components of the PLC PHY transceiver. For each of the functional blocks shown in Figure 2 a conceptual design model has been developed. Models are represented in a combination of Mathworks Simulink blocks and MATLAB code. Certain computationally intensive parts of models have also been developed as C functions and integrated as executable files into MATLAB/Simulink. The use of C-code was found to provide significant simulation time improvements especially for deeply nested iterations. Although MATLAB provides much of the necessary functionality through the additional communications toolbox, it was found that the majority of the components from that toolbox could not be adapted in order to support the necessary IEEE 1901 specification and therefore most of the models have been realized independently. Implementing the algorithms in MATLAB is much faster as many high-level functions that would not be readily available in a real hardware implementation may be used. This makes the iteration period for any necessary design changes at this level fairly quick. However, for many critical parts of the design it was also necessary to evaluate the performance of hardware implementations, given the limitations imposed by fixed-point arithmetic and finite word sizes. Many of those evaluations were initiated from design decisions and limitations found during the development of the detailed design.

One of the main measures of the performance of a communications system is the achievable Bit Error Rate (BER) for a given SNR. Simulation of a system with different SNR values leads to the generation of a

[1] Using models for requirements testing through simulation is referred to as verification within DO-331, but would be an analysis step according to DO-254. For purposes of this paper it will be referred to as verification.

so-called BER curve. Simulating the PHY transceiver with different parameter configurations or over different PLC channel/noise models allows a direct comparison of the performance to be made using the resulting BER curves. For example, measuring the horizontal offset between two curves in the "waterfall" region, or the region of high slope for larger SNR, allows a quantitative value in terms of SNR gained for a given optimization to be measured. Such simulations are also useful for isolating and evaluating the influence of impairments on the communication performance. The influence of clock frequency offset and drift is one example. Simulations may be run with no clock drift and with a model for clock drift and the difference in the resulting BER curves provides a quantified measure of the influence of that phenomenon. The simulation and comparison of BER curves has been used extensively throughout the development of the conceptual design models. An example of such curves and a comparison is shown in Figure 5 in which the performance of the transceiver is shown for four different reference channel models defined within the EU OPERA project [12]. These reference channels differ in the statistical characteristics of their impulse responses or, in other words, on the extent of their frequency selectivity. The simulations have been performed with an impulsive noise model based on the Middleton Class A model. The scalar value of SNR represents the average SNR over all sub-carriers. As can be seen when observing a BER near 10^-6 there is a difference in almost 4dB between the best channel (leftmost) and the worst channel (rightmost). The only prohibitive factor for BER curve simulation is the overall simulation time. In order to simulate a certain BER with a high confidence one should transmit a number of bits that is at least an order of two higher, e.g. for simulating a BER up to 10^-6 at least 10^8 bits must be sent. Even though several optimizations to simulation time have been made, simulating BER values up to 10^-6 with the overall transceiver model still may take several days.

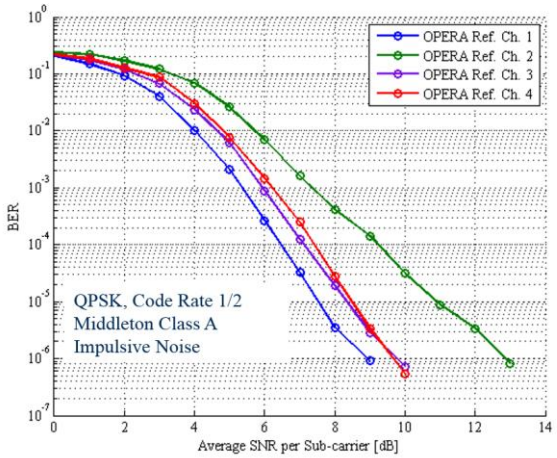

Figure 5: BER vs. average SNR per sub-carrier for different reference channels with impulsive noise

Detailed Design Models

Based on the hardware requirements and the conceptual design the next stage in the design cycle was the realization of detailed design models. Rather than using the traditional register-transfer level (RTL) representation of the detailed design by means of a hardware description language such as VHDL, a graphical representation of the hardware design has been developed in Xilinx System Generator (SysGen). SysGen provides a blockset library of commonly used DSP functions, which allows the user to develop the detailed design models within the MATLAB/Simulink environment. Making use of the advanced data generation and analysis features of this environment, bit- and cycle-accurate simulations of the detailed design can be conveniently performed. Bit accuracy is especially important for the data path portion of the design. Here, the SysGen feature of automatic and user-controlled propagation of fixed-point formats across the data path is very helpful. It allows easy evaluation of the effects of different word sizes, scaling and rounding schemes in order to find reasonable compromises between BER performance, latency and resource usage. Cycle accuracy on the other hand is crucial for the control portion of the design. It ensures that after automatic code generation of each component the overall system will function as intended.

As a graphical design entry tool SysGen shares the typical advantages and disadvantages of tools in this class. At higher architectural levels drawing block diagrams improves design productivity and provides better documentation means than textual design entry. The opposite is true for the design of low-level control structures. The possibility to include custom VHDL code into SysGen blocks provides an interesting remedy for this shortcoming, which has been used quite extensively for the PLC PHY implementation.

Verification

Three different forms of verification of the PLC PHY transceiver are performed as is shown in Figure 3. Two verification steps are performed as simulations and one as traditional testing upon the targeted hardware platform.

The basic architecture of the PHY Simulation Platform Testbench (PhySimPlatform), with which simulation verification is performed, is shown in Figure 6. It has been developed exclusively for simulation of the PLC PHY transceiver and takes advantage of the fact that both the conceptual design and detailed design models are realized within a Simulink environment. Each functional block of the PLC PHY transceiver (see Figure 2) has been developed such that the interfaces of the equivalent conceptual design and detailed design models to other adjoining blocks are compatible. For each block a Simulink variant sub-system has been defined. The use of variant sub-systems allows a parameterized selection to be made of whether the simulation shall include the conceptual or design model. Simulations may therefore be performed in which different combinations of either conceptual or detailed design models are included. This allows the input/output behavior of the detailed design models to be directly compared to the conceptual design models either on a block by block basis or across the whole transceiver chain. In that manner the behavior of the detailed design models can be verified against the expected behavior defined within the conceptual design models.

Simulations of conceptual design models are used in order to initially verify that the high level definition of the algorithms for the PLC PHY fulfill the hardware requirements. The advantage of executing the models in a simulation environment is that the influence of many real-world phenomena such as channel attenuation, noise, clock drift may be investigated in a controlled and reproducible environment. Creating such controlled environments with hardware testing is often much more challenging. The fast execution time of the MATLAB and C-code based models allows a statistical analysis through Monte Carlo type simulations to be performed.

As a second verification step the behavior of the detailed design models are tested against the conceptual design models using input/output comparison simulation. Tests are made in order to ensure that, for the same input and parameter configurations, simulations with conceptual and detailed design models provide similar output results. Execution time of the SysGen based detailed design models is rather slow meaning that these simulations are only suitable for behavioral analysis and verification and not for statistical analyses.

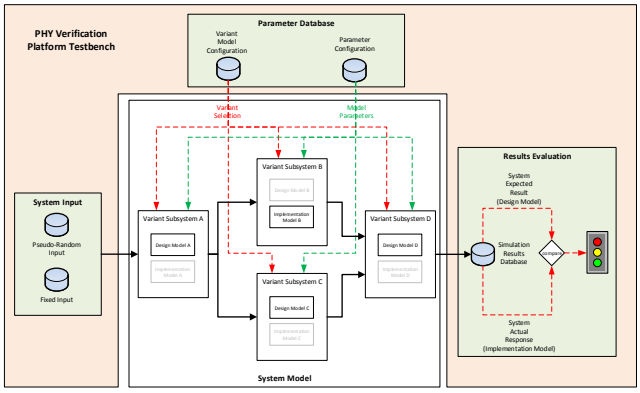

Figure 6: PHY Simulation Platform Testbench

Conclusion

The potential to completely remove the data network for an aircraft subsystem by transmitting data over the power network using Power Line Communications (PLC) presents an interesting solution for a significant reduction in the amount of wiring required in the aircraft. Many of the challenges due to the communications environment and channel have been presented. The Lucerne University of Applied Sciences & Arts has developed a PLC protocol dedicated for real-time, safety-critical applications. In order to provide robust communications over the harsh PLC communications

channel several advanced digital signal processing techniques such as Orthogonal Frequency Division Multiplexing (OFDM) and a powerful Forward Error Correction (FEC) are required. The necessity to provide design assurance has been considered in the development of the protocol.

In order to cope with the inherent complexity of designing the necessary algorithms a Model Based Design (MBD) process has been proposed. The proposed process merges concepts from DO-254 and DO-331 for the design and verification and validation processes. MBD is used both within the conceptual and detailed design with high-level MATLAB based models provided for the conceptual design and low-level detailed design models using Xilinx System Generator. Simulation of the executable models is used in order to provide an initial verification of the conceptual design models against the hardware requirements and to verify that the behavior of the detailed design models is the same as the conceptual design models. MBD has been found to provide a number of advantages including:

- Complex design may be more easily broken down into manageable design tasks
- Issues may be identified at an earlier stage in the design process
- A shorter iteration time with less effort is required to solve issues or provide optimizations
- Various aspects of the design may be investigated and tested in a controlled and reproducible environment
- The influence of important aspects under investigation may be isolated from other factors and quantitatively evaluated

Prototypes which implement the PLC protocol have been developed. The protocol is currently realized on the Xilinx Zynq System-on-Chip (SoC). The functionality of the avionics PLC solution will be demonstrated within the EC FP7 ASHLEY project using the ventilation control system as a reference application. Further next steps in the development will include the extension of the PHY simulation platform to support the simulation of VHDL code. This would support the simulation verification of the detailed design in the form of VHDL against the conceptual design. This would minimize the risk of any necessary tool qualification due to the automated code generation functionality provided by Xilinx System Generator.

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